CLAIMS

What we claim is:

1. A method of selecting a reference level from a set of possible reference levels, comprising:

using each of said possible reference levels to read a set of cells from a memory area;

determining a read error rate for each one of said possible reference levels associated with the reading of said set of cells; and

selecting a reference level from said set of possible reference levels whose read error rate is relatively low.

2. The method of claim 1, wherein said selecting comprises choosing a reference level from said set of possible reference levels resulting in the lowest read error rate.

3. The method of claim 1, wherein said selecting comprises choosing a reference level from said set of possible reference levels resulting in a read error rate that is below a predetermined threshold.

4. The method of claim 1, wherein each reference level from said set of possible reference levels is slightly different from each of the other reference voltages in said set.

5. The method of claim 4, wherein said set of possible reference levels comprises incrementally changing reference levels.

6. The method of claim 4, wherein said set of possible reference levels comprises incrementing reference levels in constant increments.

7. The method of claim 4, wherein said set of possible reference levels comprises incrementally changing reference levels in changing increments

8. The method of claim 1, further comprising repeating each of said using, determining and selecting for each verify level of said memory states.

9. The method of claim 6, further comprising using a different set of possible reference levels for each state of said memory area.

10. The method of claim 6, further comprising using a different set of possible reference levels for each state of said memory area simultaneously.

11. The method of claim 1, further comprising repeating each of said using, determining and selecting for each charge storage region of one or more memory cells.

12. The method of claim 8, wherein said repeating comprises repeating each of said using, determining and selecting for each charge storage region of one or more NROM memory cells.

13. A method of establishing a reference cell based on a selected reference voltage, comprising:

determining a read error rate associated with each possible reference voltage from a set of possible reference voltages;

selecting a reference voltage from said set of possible reference voltages resulting in a relatively low read error rate; and

establishing a reference cell based on said selected reference voltage.

14. The method of claim 13, wherein said establishing comprises:

calculating a correlation value between said selected reference voltage and each of a plurality of reference cells from a bank of reference cells; and

selecting a reference cell from said bank of reference cells having a relatively high correlation value.

15. The method of claim 14, wherein said selecting comprises choosing a reference cell from said bank of reference cells having the highest correlation value.

16. The method of claim 14, wherein said correlation value is representative of the correlation between said reference voltage and the threshold voltage of each of said reference cells.

17. The method of claim 16, wherein each of said reference cells is configured to have a slightly different threshold voltage.

18. The method of claim 17, wherein the threshold voltage of each of said reference cells is incrementally changing.

19. The method of claim 14, wherein said determining, said selecting and said establishing may be repeated for each state of a Multi Level Cell.

20. The method of claim 13, wherein said determining, said selecting and said establishing may be perform simultaneously for each state of a Multi Level Cell.

21. The method of claim 19, wherein for each repeat of said determining, said selecting and said establishing a distinct set of reference voltages is used.

22. The method of claim 13, wherein said establishing comprises adapting an offset circuit such that an effective gate voltage of the reference cell in combination with an offset value may be substantially equal to said selected reference voltage.

23. The method of claim 21, wherein said adapting comprises:

receiving an input signal to be associated with said selected reference voltage;

processing said input signal to determine an offset value associated with said selected reference voltage; and

offsetting gate voltage to be applied to the reference cell in accordance with said offset value.

24. The method of claim 23, wherein said processing comprises calculating said offset value to indicate to said offset circuit to offset an input gate voltage by said offset value, such that the effective gate voltage to be applied to said reference cell is substantially equal to the reference voltage of said reference cell.

25. The method of claim 24, wherein said offsetting comprises offsetting an input gate that is substantially equal to said selected reference voltage,

such that said effective gate voltage is substantially equal to the threshold voltage of said reference cell.

26. The method of claim 13, wherein said establishing comprises programming said reference cell such that the threshold voltage of the reference cell is substantially equal to said selected reference voltage.

27. The method of claim 26, wherein said programming comprises programming said selected reference voltage into said reference cell.

28. The method of claim 27, wherein said programming comprises programming one of a set of preselected programming values into said reference cell.

29. A method of operating a memory array based on a selected reference voltage, comprising:

determining a read error rate associated with one or more possible reference voltages from a set of possible reference voltages;

selecting a reference voltage from said set of possible reference voltages resulting in a relatively low error rate;

establishing a reference cell based on said selected reference voltage; and

operating said memory array using said established reference cell.

30. The method of claim 29, wherein said operating comprises reading at least one memory cell from said memory array using said established memory cell.

31. The method of claim 29, wherein selecting a reference voltage from the set of possible reference voltages is done prior to determining a read error rate for all of the possible sets of reference voltages.

32. The method according to claim 31, wherein the first reference voltage associated with an error rate below a predefined threshold value is selected.

33. The method according to claim 29, wherein the cell operated is selected from the group consisting of Nitride Read Only Memory ("NROM"), NROM Multi-Level Cell ("MLC"), Floating Gate MLC, and Dual Charge Storage NROM, and Dual Storage Area NROM MLC.

34. The method according to claim 29, further comprising storing the error detection rates in close proximity to the memory cells.

35. The method according to claim 29 further comprising storing the selected reference values in close proximity to the memory cells.